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Side-channel Analysis for Hardware Trojan Detection

Hardware Trojans pose a critical security risk by embedding malicious functionality that can evade design-time verification and remain dormant until activated. This ongoing project investigates side-channel analysis as a non-invasive approach for detecting hardware Trojans in FPGA-based systems, with a particular focus on electromagnetic (EM) emissions. An AES-128 encryption core is implemented on a Zynq XC7Z020 FPGA platform and serves as the baseline for experimental evaluation. The EM emission characteristics of the Trojan-free design are first measured and statistically characterized under controlled operating conditions. Representative hardware Trojans, including leakage-based and trigger-activated designs, are then integrated into the AES core to emulate realistic attack scenarios. EM measurements are collected both before and after Trojan insertion, and deviations in spatial and temporal emission patterns are systematically analyzed. Multiple side-channel analysis techniques, such as statistical feature extraction, and anomaly detection, are employed to distinguish Trojan-infected designs from trusted implementations. This work aims to contribute an experimental framework and effective detection methodology for identifying hardware Trojans on FPGA platforms.

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