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Van der Waals Integration of Semi-Metallic PdSe₂ Contacts for High-Performance n-type WS₂ Field Effect Transistors

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Two-dimensional transition metal dichalcogenides (TMDs) show immense potential for next-generation nanoelectronics and optoelectronics, owing to their atomic-scale thickness and compatibility with van der Waals (vdW) integration. Consequently, TMDs have become central to emerging technologies such as neuromorphic computing, high-speed photodetectors, and superconducting quantum circuits. However, a critical bottleneck remains the high contact resistance at the metal-semiconductor interface, often caused by Fermi level pinning and substantial Schottky barrier heights. This interface degradation leads to severe resistive power loss and limits device scalability. To address this, we investigate the efficacy of few-layer, semi-metallic palladium di-selenide (PdSe₂) as a van der Waals contact interlayer. We fabricated field effect transistors (FETs) utilizing n-type tungsten disulfide (WS₂) as the semiconducting channel and PdSe₂ as the source/drain terminals. We evaluated performance metrics, including carrier mobility and contact resistance, using the transfer length method across varying channel lengths. Temperature-dependent transport measurements were performed to determine the Schottky barrier height. Preliminary results indicate that PdSe₂ contacts significantly improve carrier injection compared to traditional metals. The improved performance is attributed to the favorable band alignment between the semi-metallic PdSe₂ and n-type WS₂. This work highlights the promise of PdSe₂ as a scalable, low-resistance contact material for high-performance 2D electronics.

Academic or Professional Status

Postdoctoral Researcher / Research Scientist

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